Appl. No. 10/734,195

Date of Response: December 5, 2005

## **Listing of Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended):

A multichip module structure, at least comprising:

a first multichip module substrate, comprising:

an <u>a</u> semiconductor substrate having a first surface and a second surface;

an insulating layer being on said first surface;

a multilayer interconnection structure being on said insulating layer and having a third surface having a plurality of first bonding pads and a fourth surface having a plurality of second bonding pads and contacting on said insulating layer;

a plurality of conductive plugs penetrating said semiconductor substrate and said insulating layer and electrically connecting to said second bonding pads respectively;

a plurality of third bonding pads being on said second surface and connecting to said conductive plugs respectively; and

a plurality of chips being on said second surface and electrically connecting to said third bonding pads.

Claim 2(original):

The multichip module structure according to claim 1, wherein said multilayer interconnection structure includes at least `one integrated circuit device.

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Claim 3(currently amended):

The multichip module structure according to claim 1, wherein said semiconductor substrate has a thickness between 10 to 500 micron meter.

Claim 4 (original):

The multichip module structure according to claim 1, wherein said chip is an active chip.

Claim 5 (original):

The multichip module structure according to claim 4, wherein said active chip is mounted on said second surface by flip-chip type.

Claim 6 (original):

The multichip module structure according to claim 1, wherein said chip is a passive chip.

Claim 7 (original):

The multichip module structure according to claim 1, wherein said chips individually and electrically connect to said third bonding pads.

Claim 8 (currently amended):

The multichip module structure according to claim 1, wherein said plurality of chips comprise a first active chip mounted on said first multichip module substrate second surface by flip-chip type, and at least one chip electrically connecting and stacking on a backside of a said first active chip.

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Claim 9 (original):

The multichip module structure according to claim 8, wherein said at least one chip comprises a second active chip mounted on said backside of said first active chip by flip-chip type.

Claim 10 (original):

The multichip module structure according to claim 8, wherein said at least one chip comprises a passive chip.

Claim 11 (original):

The multichip module structure according to claim 1, further comprising a second multichip module substrate on said third surface, wherein said second multichip module substrate has a same structure as said first multichip module substrate.

Claim 12 (currently amended):

The multichip module structure according to claim 1, wherein said multichip module structure is further electrically connected with a eircuit board package substrate on said third surface.